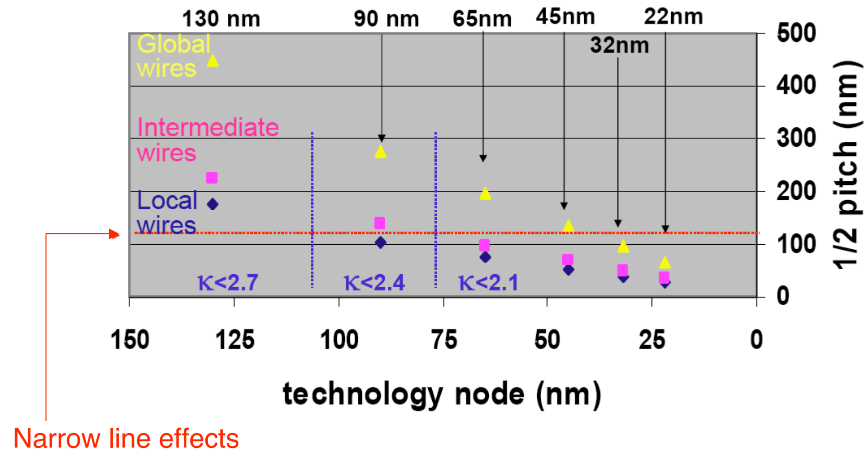
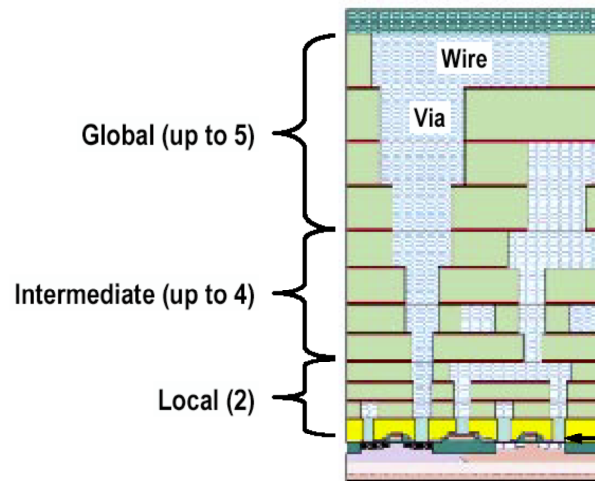
Deposition & Planarization

Scaling of interconnects requires more metal layers with reduced interconnect pitch. The height of metal has to be increased. The increased aspect ratio between the metal lines will increase dramatically the problem of step coverage.





The interconnect topography can cause problems in step coverage and lithography.

Depth of Focus in Lithography

From optics:

$$F_{number} = \frac{f}{D} = \frac{\text{focal length of lens}}{\text{diameter of lens}}$$

$$\text{Resolution} = 1.22\lambda F_{number}$$

$$\text{Depth of field} = \pm 2\lambda F_{number}^2$$

Example:
We need to resolve 0.1 μm lines and spaces
If λ = 180 nm for the light source, we need F_{number}=0.45 to resolve 0.1 μm features

Depth of field = $\pm$ 0.07 μm

Resolution can be increased but the depth of field will decrease.

Gate stack for a 0.1 μm MOS transistor is shown in Fig. 2. It will be difficult to define features simultaneously at the top and the bottom surfaces of this type of structure.

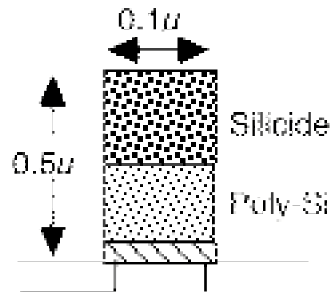
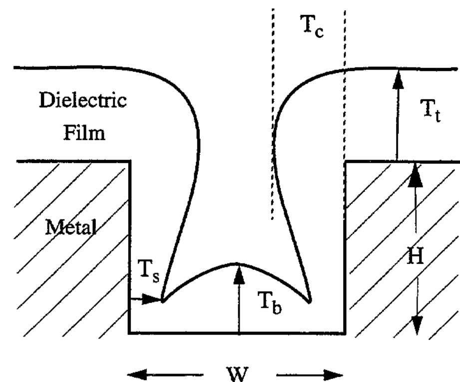


Fig. 2

Step Coverage



$$\text{Aspect Ratio} = \frac{H}{W}$$

$$\text{bottom step coverage} = \frac{T_b}{T_t}$$

$$\text{side step coverage} = \frac{T_s}{T_t}$$

$$\text{cusping} = \frac{T_c - T_s}{T_s}$$

Fig. 2 Step coverage definitions. Poor step coverage results from different deposition rates in different parts of a nicrostructure.

The profile of the thin films deposited by any of the CVD or PVD techniques depend upon:

1. Equipment configuration
2. Deposition method (LPCVD, PECVD, PVD)
3. Reaction chemistry
4. Reactant transport mechanism

Deposition Techniques

Chemical vapor deposition (CVD): Deposition occurs as a byproduct of a chemical reaction in vapor phase.

Physical vapor deposition (PVD): Deposition occurs as a byproduct of a physical process, such as, evaporation from a source followed by condensation on another surface.

Chemical Vapor Deposition Systems

Various chemical vapor deposition (CVD) techniques are commonly used for semiconductor processing. Deposition temperatures vary from 100°C to 1000°C, and pressure ranges from atmospheric to the milliTorr regime. The energy for the reaction can be thermal, photochemical or electrical (for plasma processes). For each of these techniques there is a wide range of reactor configurations which have been used.

Atmospheric Pressure Chemical Vapor Deposition (APCVD)

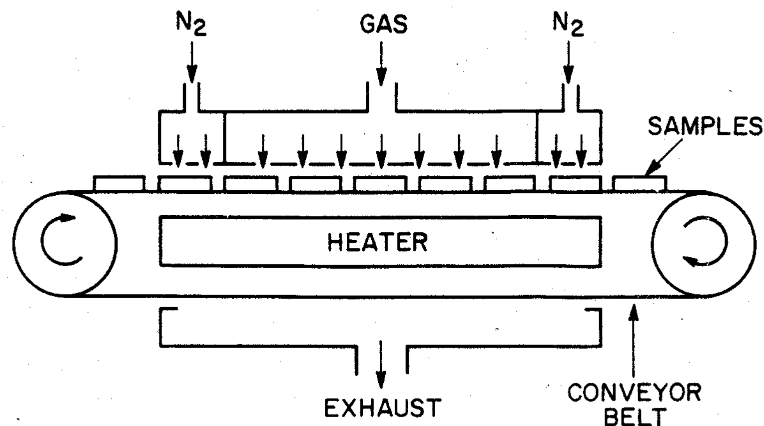


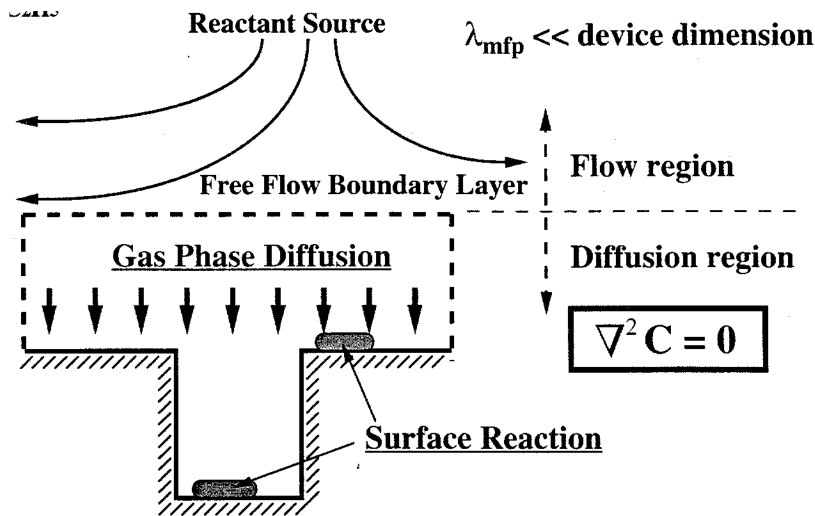
Fig. 5. Continuous Flow Atmospheric Pressure Reactor

In the early days of semiconductor processing atmospheric pressure reactors were used to deposit silicon and dielectric films. The advantage of deposition at atmospheric pressure is the simplicity of the reactor design and that high deposition rates are obtained. Although several different reactor geometries were used, the operating principle is the same in all these reactors. The wafers are put on a hot susceptor and reactant gases flow over the susceptor. The susceptor is heated by using high-intensity lamps, radio frequency induction, or dc electric current (resistive) heating. These atmospheric pressure reactors have low throughput, require excessive wafer handling during wafer loading and unloading and have poor thickness uniformity (>- 10%) across the wafer.

To overcome some of these disadvantages, continuous throughput atmospheric pressure reactors were developed. In these reactors the wafers are carried through the reactor on a conveyor belt and are heated by convection. Also, there is a more uniform flow of the reactant gases across the wafer surface. These reactors have high throughput, good uniformity and the ability to handle large diameter wafers. The main disadvantages of this type of reactor are that they required frequent cleaning and that particles formed on the reactant dispenser head wind up on the wafers which impaired process yield and device reliability.

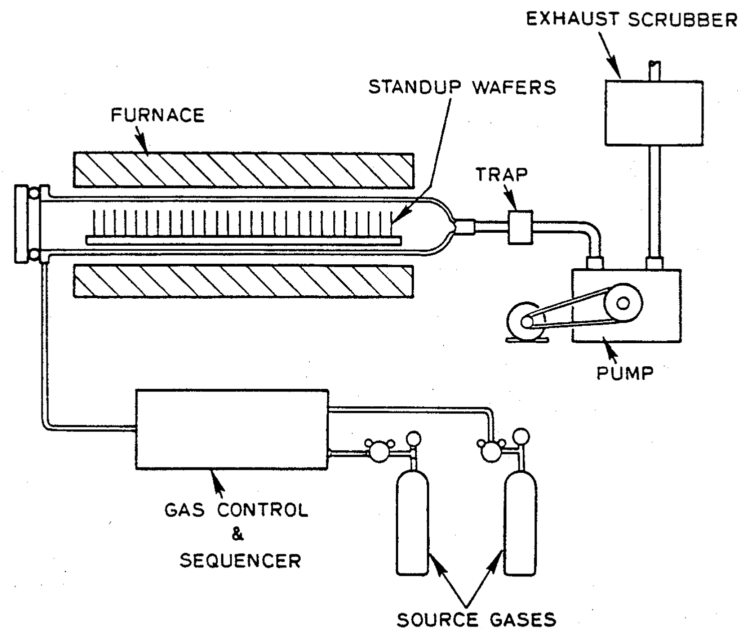
Transport of reactants to the surface at atmospheric pressure

Mean free path in the gas phase is much smaller than the dimensions of features on a wafer. Gas-gas collisions control the transport.



Mean free path in the gas phase is much larger than the dimensions of features on a wafer. Surface collisions and re-emission control the transport.

Low Pressure Chemical Vapor Deposition (LPCVD) Reactors



$$Dep.\,rate = \frac{kh}{k+h} \cdot \frac{N_g}{n}$$

$$where\ the\ mass\ transfer\ coefficient\ h \propto Diffusivity \propto \frac{1}{pressure}$$

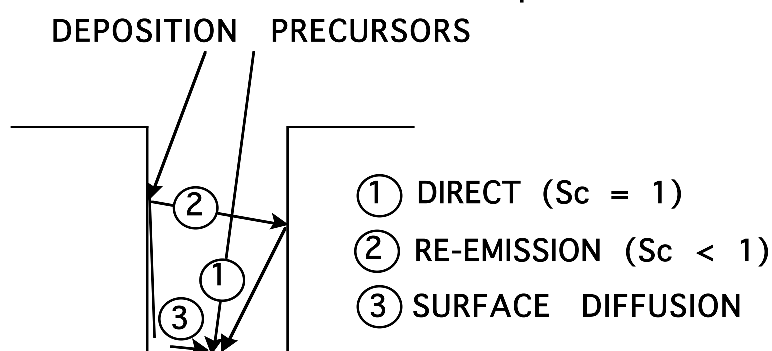
Where k is the surface reaction rate constant and N_g/n gives the concentration of the depositing species.

Low pressure chemical vapor deposition reactors were developed to overcome the disadvantages of the high pressure systems discussed above. One of the difficulties in the cold wall systems (where only the susceptor holding the wafer is heated) described above is maintaining a uniform temperature across the wafer surface. This can be overcome by putting the entire reaction chamber in a furnace maintained at a uniform temperature as in the case of standard resistance heated hot wall tubular furnaces. A large number of wafers can be stacked closely in these furnaces and good uniformity across the wafer and wafer to wafer film thickness can be achieved if they are operated at very low pressures and in the surface reaction limited regime. The transport of the reactant gases to the wafer surface in these reactors is by gas phase diffusion. At very low pressures the diffusion coefficients of the gas phase species is very large and if the process is surface reaction limited, there is an approximately uniform distribution of the reactive gas phase species throughout the reaction chamber, which results in a uniform fllm deposition.

Figure above gives the schematics of a hot-wall, low pressure chemical vapor deposition reactor used to deposit polycrystalline silicon, silicon dioxide and silicon nitride. The reactor consists of a quartz tube heated by a resistance heated furnace to maintain a uniform temperature along the reactor. Gases are introduced in one end and pumped out from the other end of the reactor. The operating pressures range from 0.25 Torr to 2 Torr and temperatures range from 300 to 900°C, and gas flow rates range from 100 to 1000 sccm. A large number of wafers (~ 100) are stacked vertically, perpendicular to the gas flow, in a quartz holder. The inlet gases may undergo homogeneous gas phase reactions to produce the deposition precursors which are transported to the wafer surface by gas-phase diffusion. Excellent film uniformities ($\pm$5%) are obtained in these reactors. Although these reactors have lower deposition rates, it is found that this is more than compensated for by the high wafer capacity.

With increasing wafer size, the film uniformity in the low pressure batch reactors tends to decrease. It should be mentioned that the future trend is towards single wafer processing systems instead of the batch system described above. This is because of the increasing wafer sizes (8" or higher), and the development in technology to achieve better film uniformity and higher deposition rates in modern single wafer reactors.

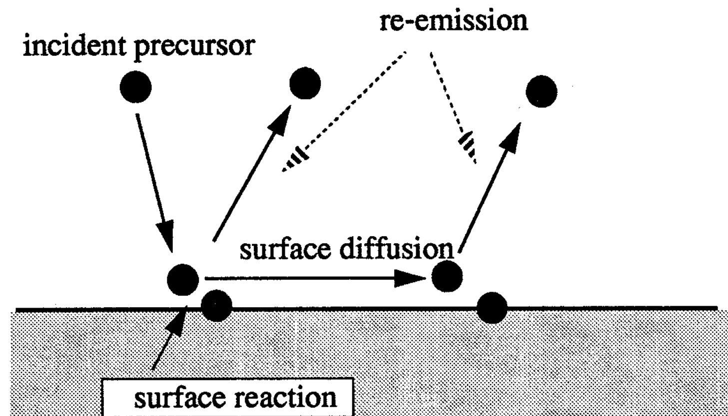
Transport of reactants to the surface at low pressures



In most applications surface diffusion has been found to be negligible.

Sticking Coefficient

S_C - Reactive sticking coefficient is the probability of an incident deposition precursor



$$S_c = \frac{\Gamma_{incident} - \Gamma_{re-emission}}{\Gamma_{incident}} = \frac{\Gamma_{reaction}}{\Gamma_{incident}}$$

Typical deposition pressures

Low pressure CVD (LPCVD) ~ 0.5 Torr
PECVD 0.5 m Torr - 1 Torr
Sputtering 1 - 20 x 10^{-3} Torr

Mean Free Path $\lambda_m = \frac{1}{260P}$ cm where P is the pressure

Pressure(torr)	760	1	0.1	.01	0.001
λ_m (Cm)	6.26 x 10^{-6}	4.5 x 10^{-3}	4.5 x 10^{-2}	0.45	4.5

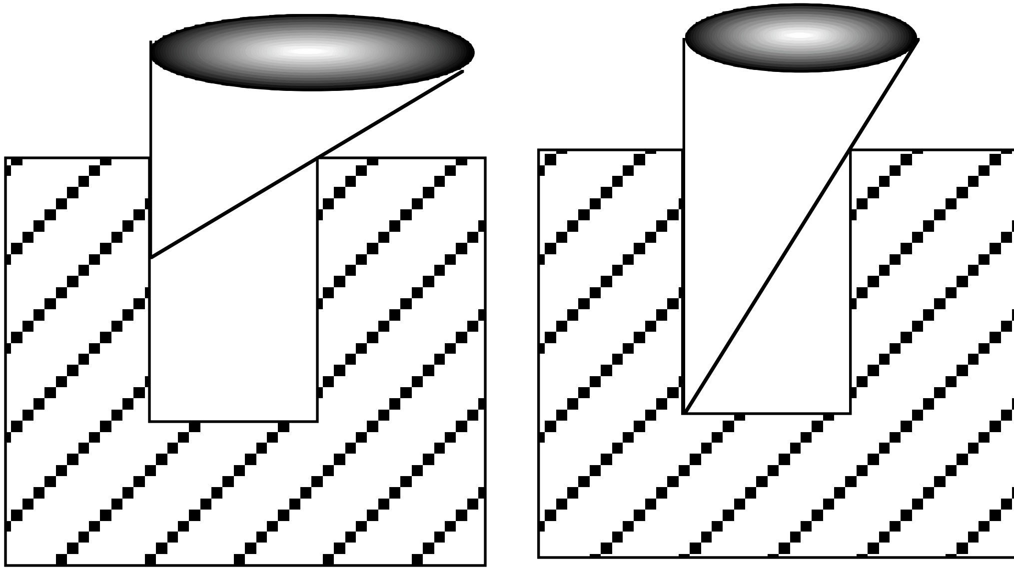
Particle Transport at Low Pressures

Above Wafer --- Mean Free Path << Chamber Dimensions
Viscous Flow --- Gas-gas Collisions

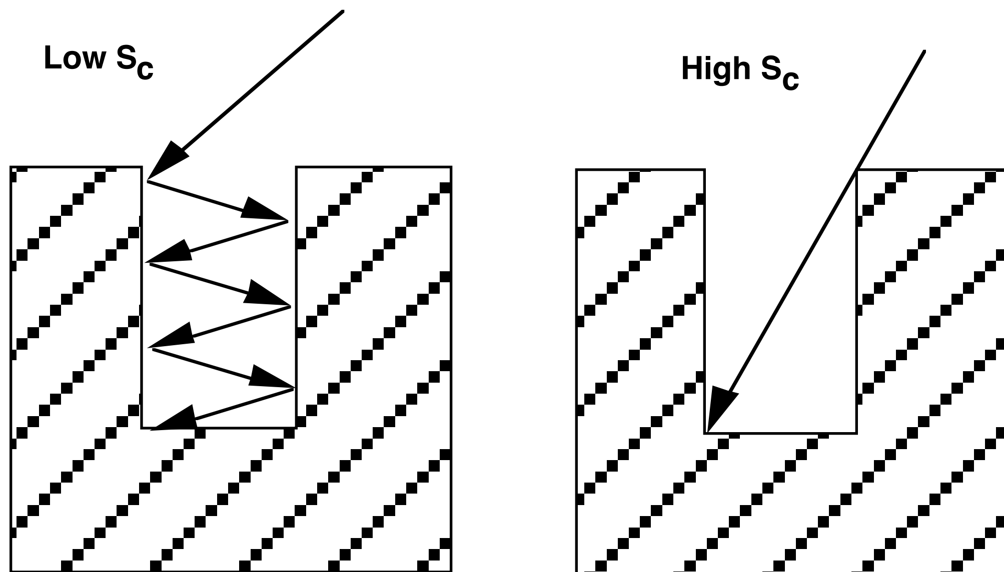
Near Water Surface ... Mean Free Path >> Device Dimensions
Molecular Flow -- Gas - wafer surface collisions

Since the mean free path for LPCVD and PECVD 10 μ m and for sputtering a few cm we can ignore collisions between the gas particles when they are inside a via or a trench like structure. The only collisions are those with the surface of the wafer.

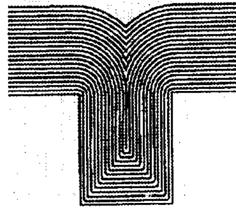
Shadowing of the direct flux by the walls reduces the flux at the bottom corners of a via or a trench resulting in thinner deposition.



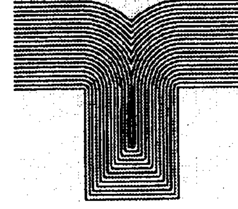
Lower sticking coefficient increases the number of bounces and hence increases the probability of deposition precursors reaching the bottom. Hence, step coverage is better for lower S_C.

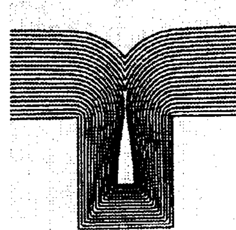


APCVD **LPCVD**

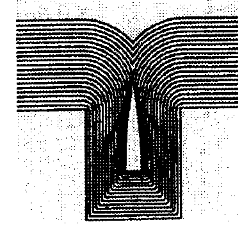


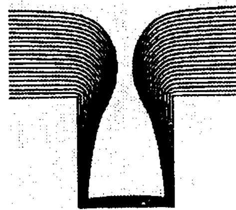
$\alpha = 100$ $S_c = 0.007$



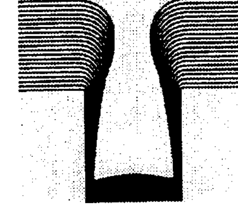


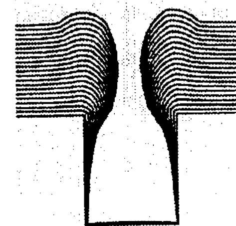
$\alpha = 10$ $S_c = 0.07$



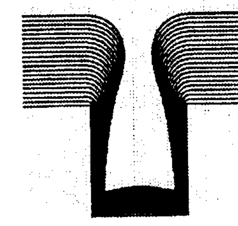


$\alpha = 1$ $S_c = 0.7$

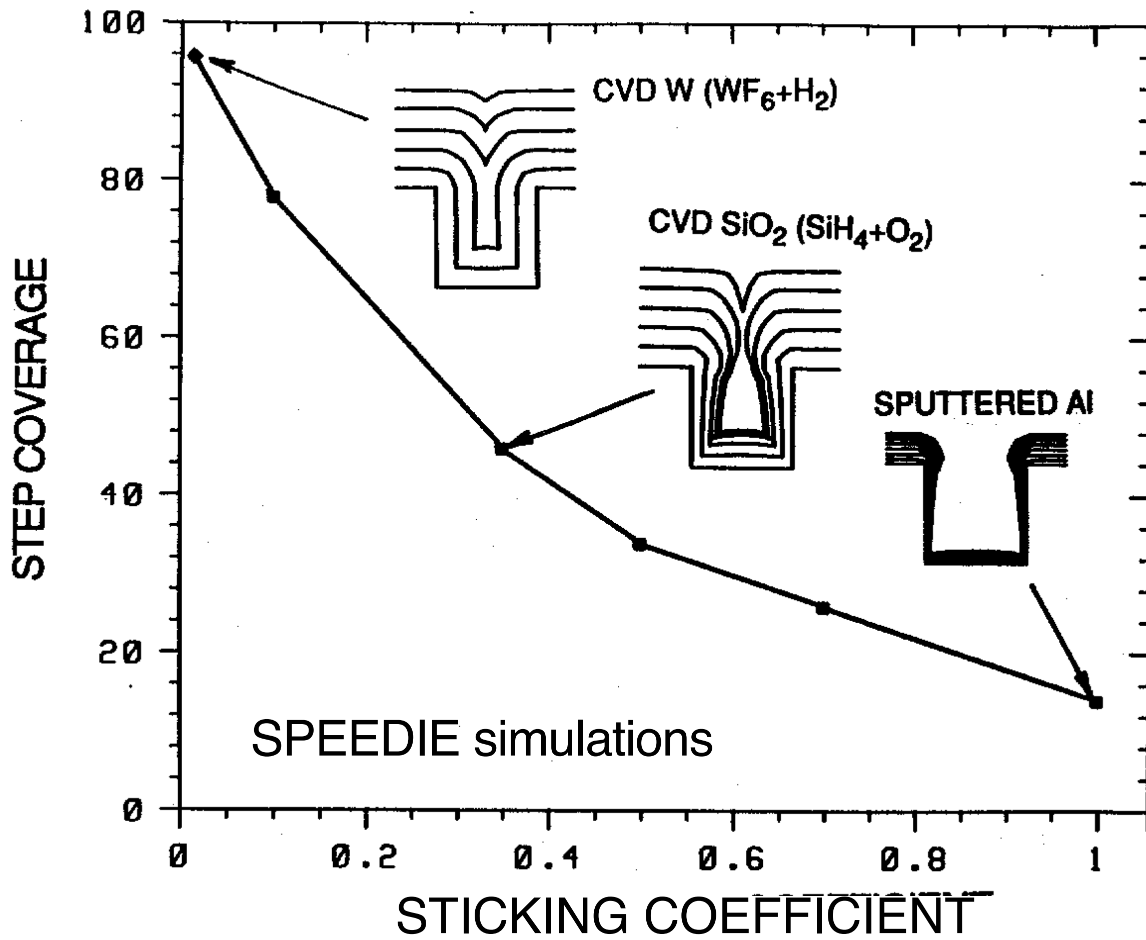




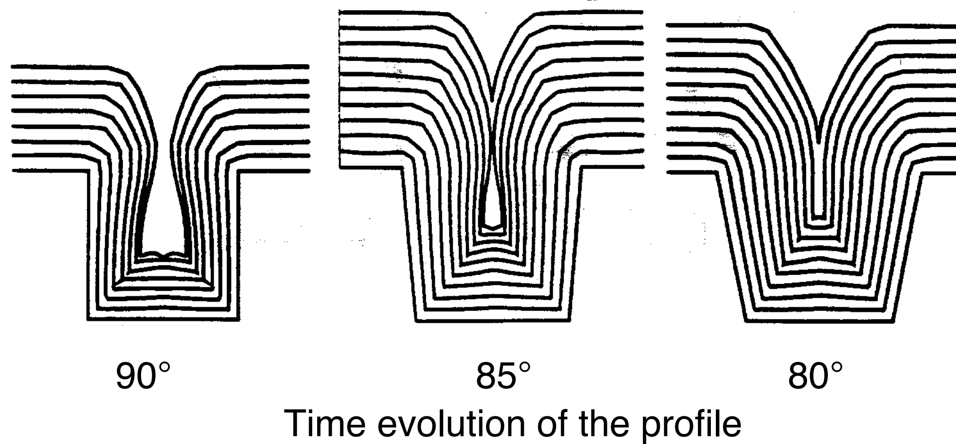
$\alpha = 0.25$ $S_c = 1$



$$\alpha = \frac{D}{KS} = \frac{\textit{Gas phase diffusivity}}{\textit{Surface reactivity} \bullet \textit{Diffusion layer thickness}}$$



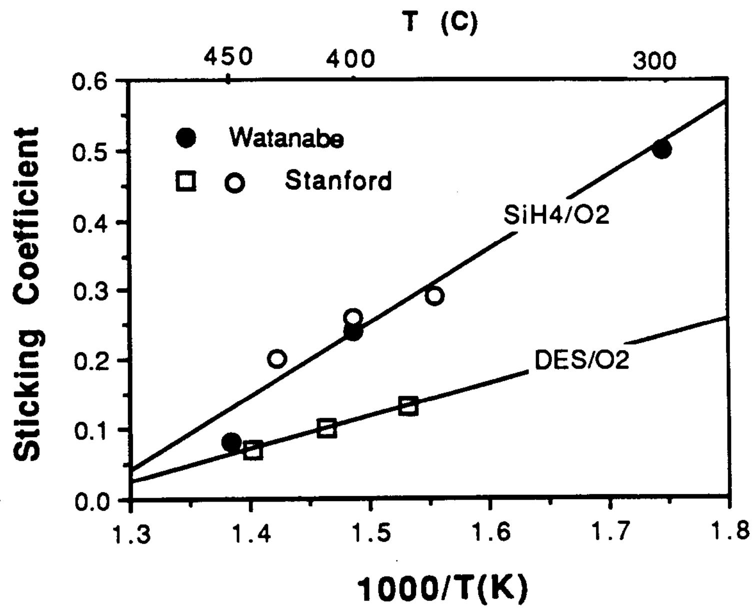
Step coverage can also be improved by changing the slope of the walls. But this may result in an area penalty.



90° 85° 80°

Time evolution of the profile

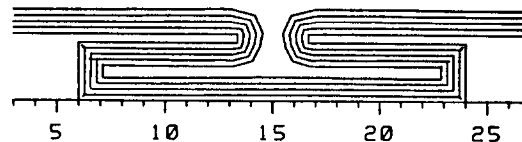
Different lines show time evolution of the profile as simulated by the deposition and etch simulator SPEEDIE



K. Watanabe et al, J. Electrochem. Soc., 137, p1222, 1990

Material	*Source*	*Temperature* °C	S_c
PSG	SiH_4/ O_2/ PH_3	400	0.35
SiO_2	SiH_4/ O_2	400	0.26
SiO_2	DES/ O_2	380	0.1
SiO_2	TMCTS/ O_2	560	0.04
SiO_2	TEOS/ O_2	700	0.04
Poly–Si	SiH_4	620–900	<0.01
W	WF_6/ H_2	350–500	<0.01

-PCVD of tungsten in a cavity showing ex step coverage.



Plasma Enhanced Chemical Vapor Deposition

One of the important limitations of LPCVD is that it requires high deposition temperatures, which may be incompatible with the other process steps,e.g., deposition on an aluminum film. In PECVD, the homogenous gas phase reactions are initiated by neutral collisions with the non-equilibrium energetic electrons produced by a rf plasma instead of thermal energy. Thus the deposition precursors can be produced at much lower temperatures by these homogenous reactions. Furthermore, ion bombardment makes the surface more reactive by creating more dangling bonds (active sites) and/or supply instantaneous energy at the surface for the heterogenous reaction to take place. In general, PECVD can be carried out at a much lower temperature than LPCVD. Moreover the deposition rate is found to be higher in PECVD than in LPCVD.

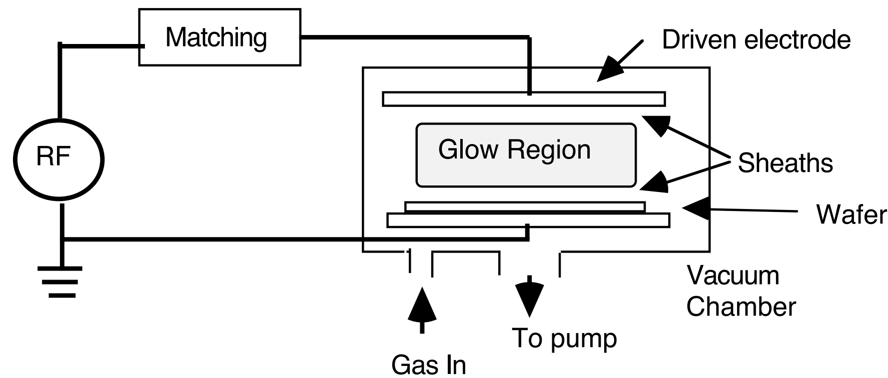


Fig 7. Parallel plate plasma enhanced chemical vapor deposition reactor

There are a number of different reactor configurations used for PECVD but the physical principle is the same in all cases. Figure 7 shows the schematic of a cold wall, parallel plate plasma deposition reactor which is very similar to an etching reactor. The chamber consists of two electrodes, one of which is grounded and the other is powered by a rf source. The wafers are placed on the grounded electrode and are heated from below to the desired temperature by resistive heaters or high-intensity lamps. The reactant gases are introduced at the outer periphery, they flow radially towards the center from where they are pumped out. A plasma is generated between the electrodes by the rf voltage applied across the electrodes. The electrode spacing is about 5 - 10 cm and the operating temperature and pressure are - 400°C and 0.1 - 5 Torr respectively. Homogenous reaction between the reactant gases is initiated by the electrons produced in the plasma. The ions are accelerated towards the electrodes due to the self bias voltage between the plasma and the electrode. These energetic ions bombard the surface, making it more reactive, leading to higher deposition rates.

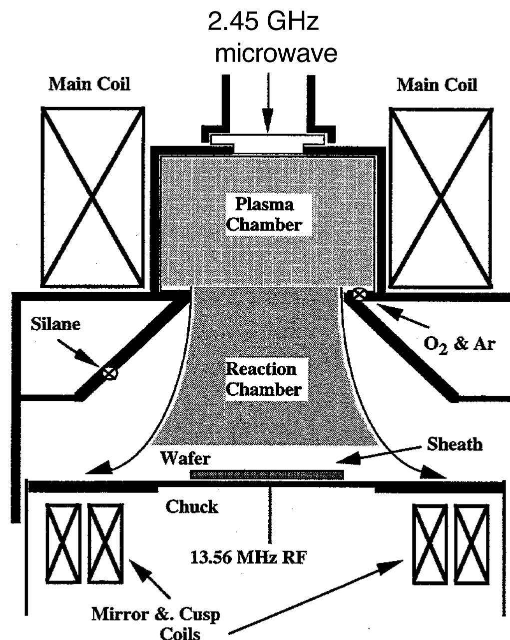


Fig. 8. Electron Cyclotron Resonance (ECR) high density plasma CVD system.

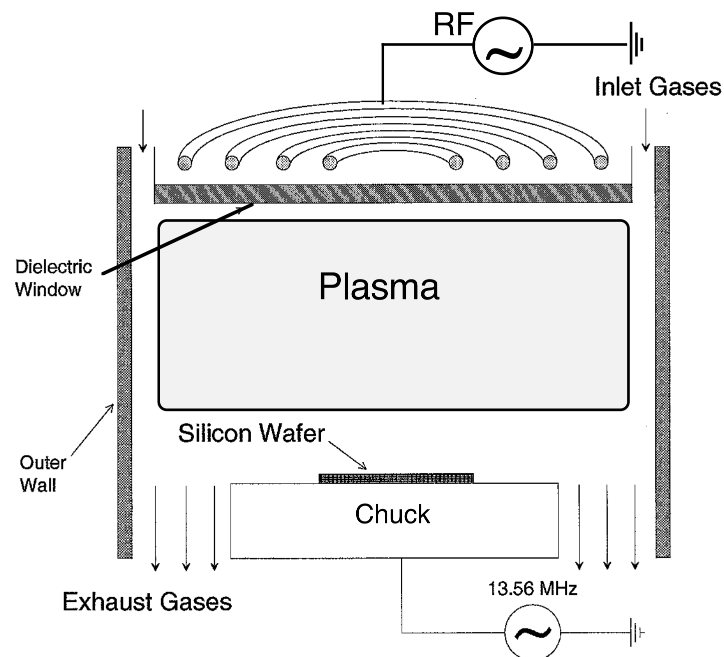
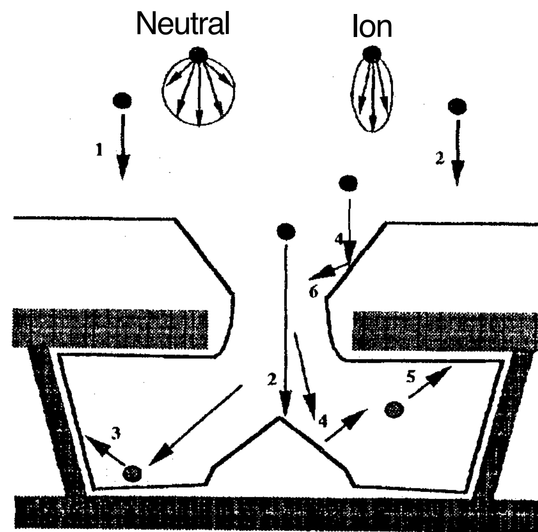


Fig. 9. Inductively coupled high density plasma CVD system.

Fig. 8 and 9 show high density plasma CVD systems. These are very similar to the systems used for etching. Unlike other CVD systems there is no intentional heating. The major difference between the HDP and the parallel plate systems is the independent energy sources for plasma generation and controlling ion energy by biasing the wafer electrode. The high energy ions can sputter etch the wafer. This feature can be used to improve the step coverage to the extent of gap filling in a high aspect ratio gap. The energy imparted by the ions is sufficient to raise its temperature to 300-400°C. Generally the wafers have to be cooled to ensure that the temperature is not too high.

Possible Surface Processes in Ion Induced Deposition

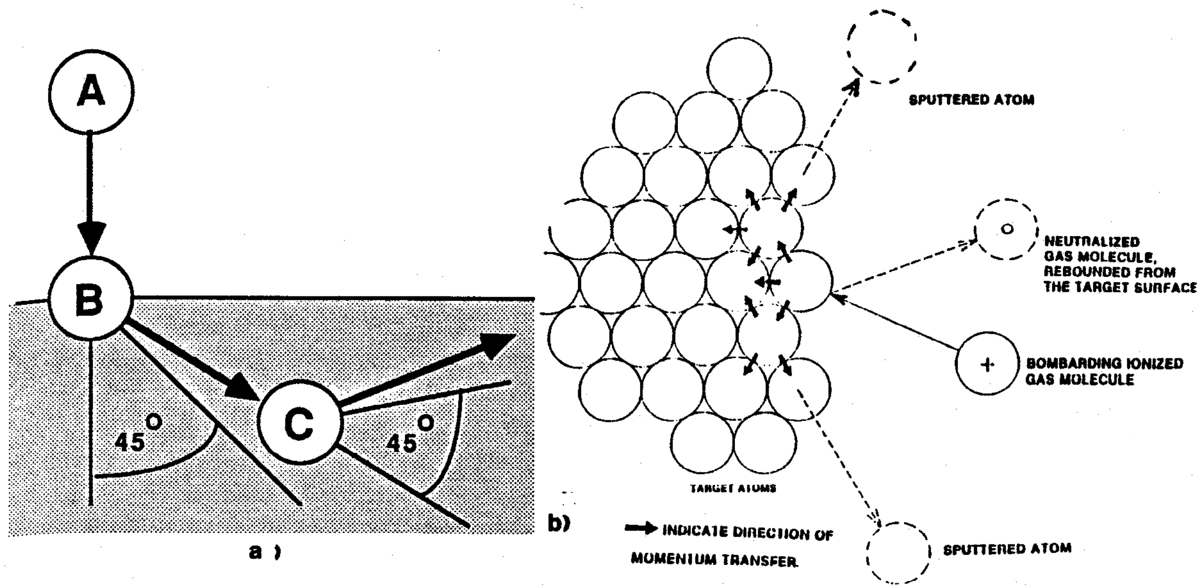
The surface processes can be understood by studing deposition in a cavity like structure with an overhang.



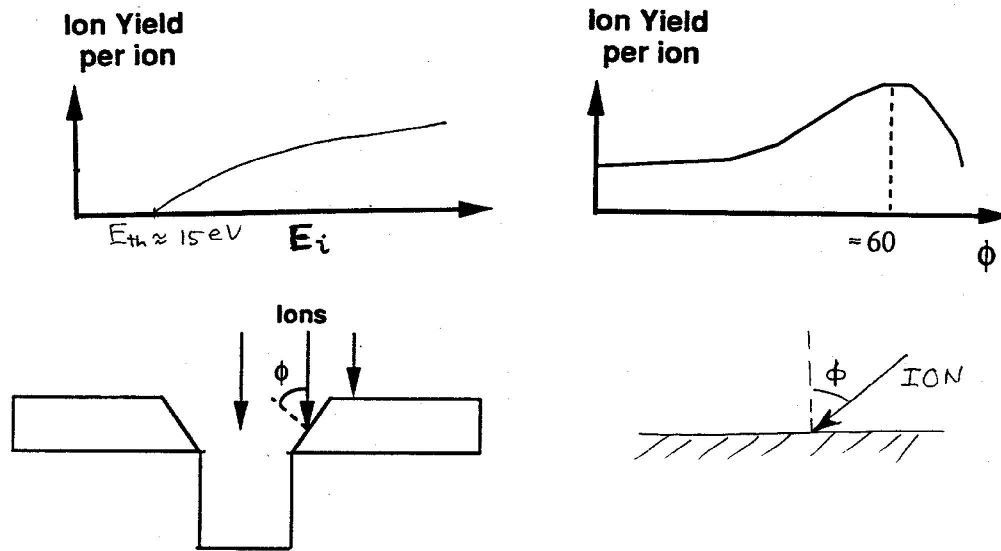
1. Direct deposition from neutral particles
2. Ion-driven direct deposition
3. Indirect diffuse re-emission
4. Resputteriuig of deposited material
5. Redeposition of sputtered material
6. Specular reflection

Sputter Etching Mechanisms

Physical etching involving momentum transfer
--"Atomic Sandbasting"

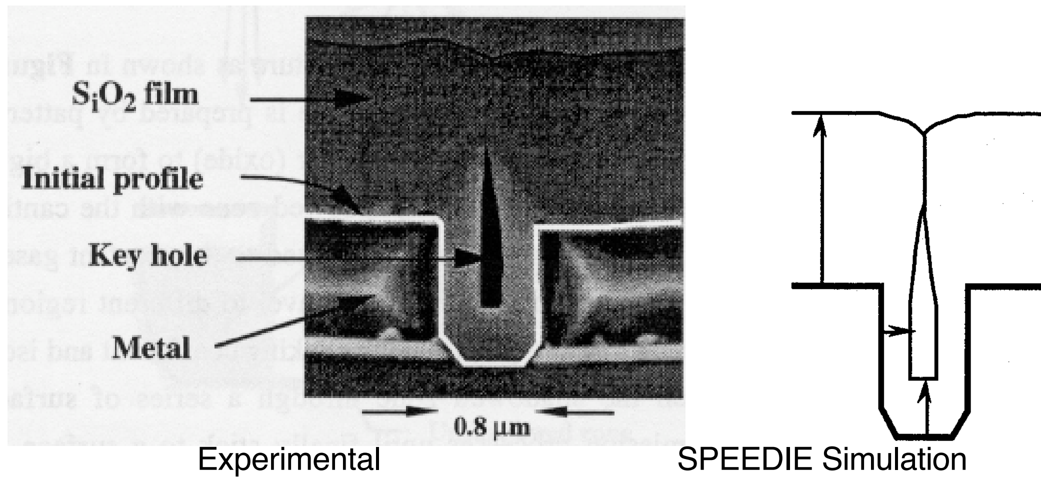


- Energy and angle dependent



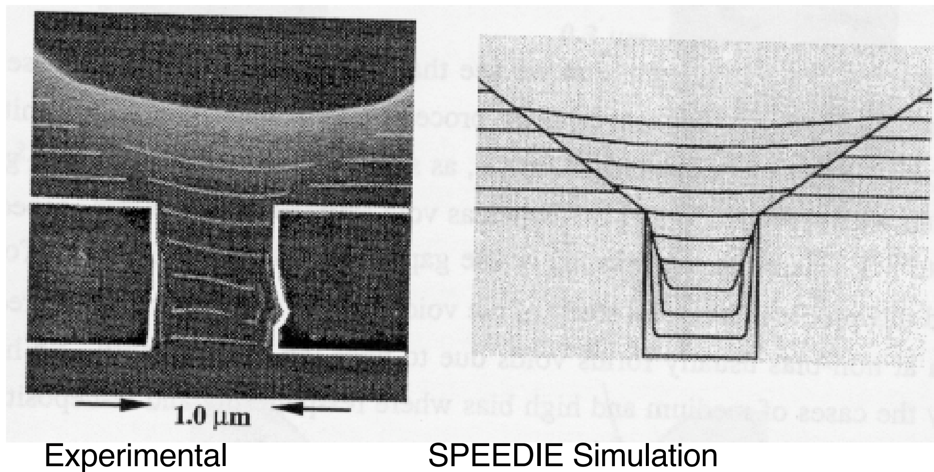
Deposition profile in parallel plate plasma CVD

Only direct deposition from neutral particles and ion-driven direct deposition take place. The deposition rate on side walls is much less than at the bottom, resulting in a key hole like void formation.



Experimental SPEEDIE Simulation

<u>Deposition profile in high density plasma CVD</u>



Experimental SPEEDIE Simulation

In HDP there are energetic ions because of the bias resulting in both deposition and sputter-etching taking place. The relative rates of each process depend upon the ion flux, angular distribution and ion energy.

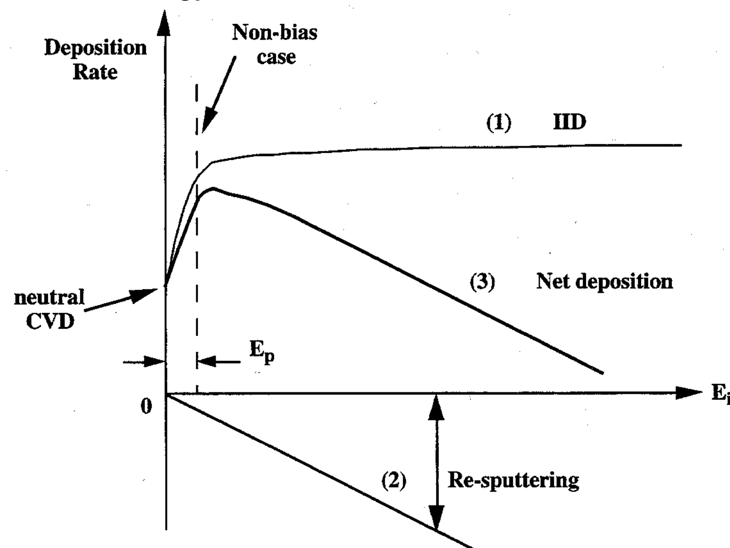
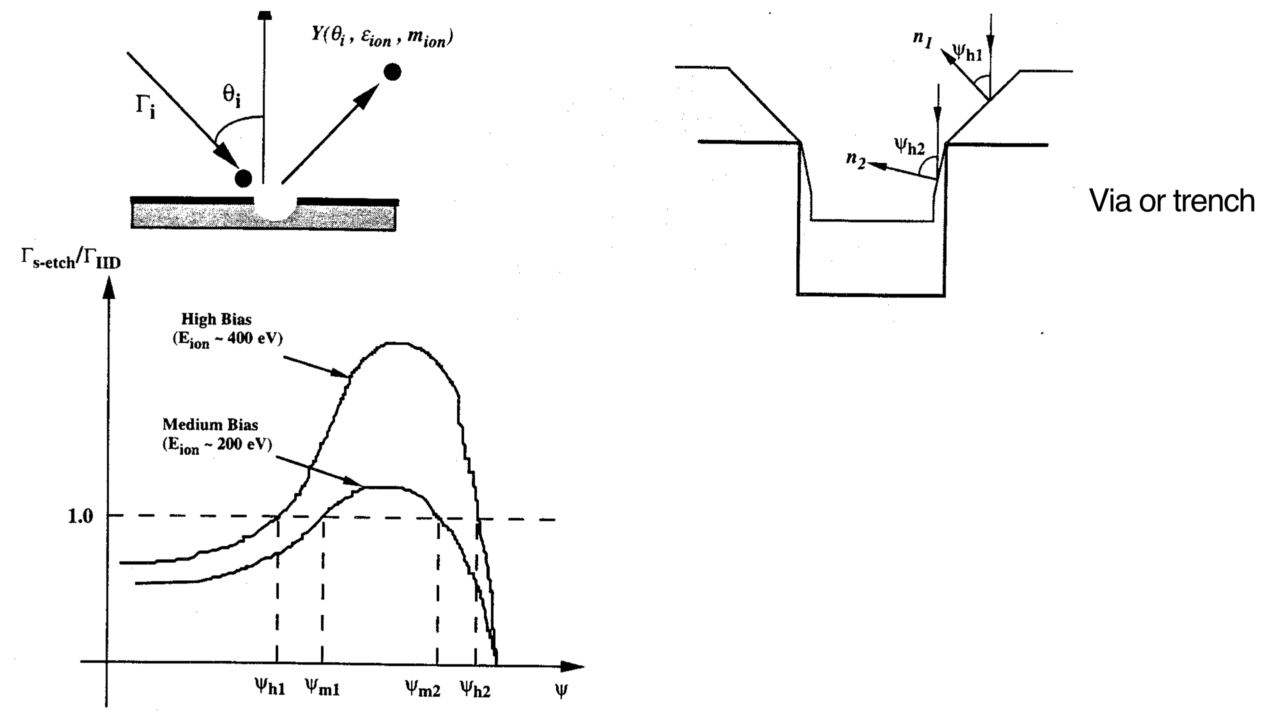


Fig. Deposition and sputter-etch rates on a flat surface

Facet formation due to sputter yield in HDP due to the bias applied to the wafer resulting in energetic ions hitting the surface.



By controlling the facet formation and deposition rates the void formation can be avoided even in high aspect ratio structures.

Physical Vapor Deposition (PVD)

Mostly used for metal deposition

1. Evaporation
    - Filament
    - Electron gun
2. Sputtering

Evaporation

The source of condensable reactive species in physical vapor deposition is either by evaporation or sputtering. In PVD by evaporation, heat is applied to the source of film material causing its evaporation. The evaporated particles get transported to the wafer surface where they condense to deposit the required film. Evaporation is carried out under high vacuum conditions (~ 5×10^{-7} Torr). There are various methods used for the evaporation of the source metals such as resistive heating, electron beam and inductive heating. In resistively heated sources, small strips of the source metal are put on a wire of low vapor pressure metal (e.g. W) which is resistively heated. In electron beam evaporation, a stream of high kinetic energy (5 - 30 key) electrons is directed at the material to be evaporated. The kinetic energy of the electrons is transformed into thermal energy upon impact and supplies the heat required to evaporate the target material. In inductive heating evaporation, the energy for evaporation is supplied by an rf induction heating coil

surrounding the crucible containing the evaporation source. The mean free path of the evaporated molecules during PVD by evaporation is much larger (~ 100 m) than the reactor dimensions, as such the transport of these molecules in the reactor is collisionless ,i.e., is in line of sight.

Though PVD by evaporation has a good deposition rate (e.g. 0.5 μmlmin. for Al) and low surface damage and impurity incorporation, it has some important limitations:

i) Accurately controlled alloy compositions are difficult to obtain.
ii) Filament life is very short.
iii) Film uniformity across the wafer and the step coverage is not as good as sputter deposition.
iv) There may be x-ray damage to the film if an E-beam source is used.
v) High melting point materials, e.g., tungsten cannot be as easily deposited by evaporation (especially by filament) as by sputtering.
vi) In-situ cleaning of the substrate surfaces is not possible.

Sputtering

Because of the limitations of the evaporation process, sputtering deposition is the most widely used PVD technique. Moreover, sputter deposition offers a better control of the process such as film thickness, and film properties such as grain size and step coverage. In sputter deposition highly energetic ion beams are directed against a target to dislodge (sputter) the target molecules, which are subsequently transported to the wafer surface where they condense to form the desired film. Sputter deposition is performed at moderately low pressures (2 - 100 mtorr) in an inert gas (generally argon) ambient. In reactive sputter deposition, the reactor is filled with a reactive gas which reacts with the sputtered material and deposits compound films, e.g. TiN. The energetic ions used to strike the target materials to be sputtered are generated by glow discharges.

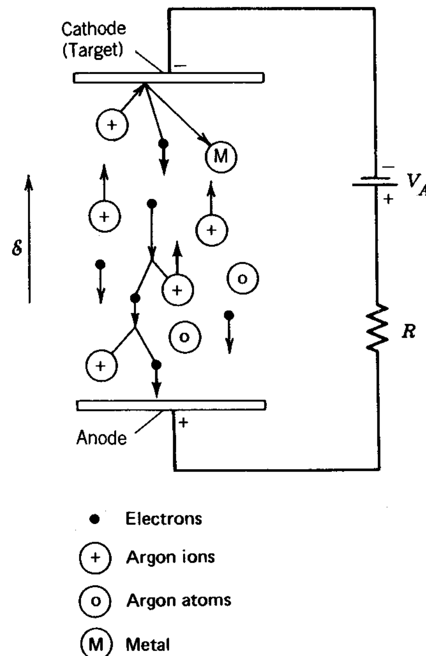


Fig. 10. A dc sputtering system

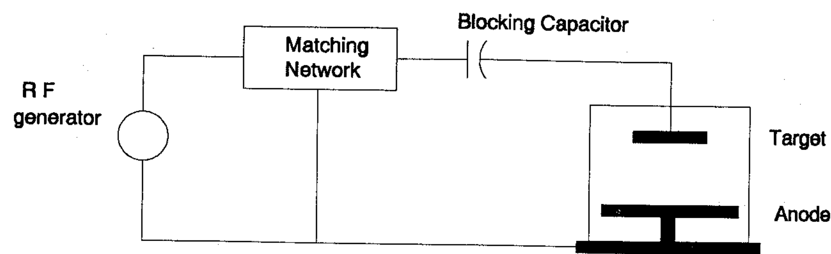


Fig.11: An rf sputtering system

The commonly used techniques for sputtering the target material are:
i) radio frequency (rf) sputtering and
ii) magnetron sputtering (rf or dc).

In a rf sputtering system, positive ions are generated by collisions of neutral species with the electrons in the plasma, which is sustained by a rf current. The ions gain energy by being accelerated towards the target due to the voltage across the plasma sheath.
Today most PVD is done by sputtering using a magnetron. For conductors a dc source is usually used, while for insulators an rf source is used. Magnetron sputtering increases the electron utilization by confining the electrons, which cause ionizing collisions, near the target surface with the help of magnetic fields. Current densities achieved in magnetron sputtering systems are much higher (10 - 100 mAlcm2) compared to rf sputtering sources (1 mAlcm2). The figure below shows a schematic diagram of a planar magnetron target. In planar magnetrons, the target surface is planar and the magnetic field is created by magnets behind the target. It is seen from this figure that half way between the magnet poles, the magnetic field (B) lines are parallel to the target face and since the electric field (E) is perpendicular to the target face, the E x B field closes on itself in this region, establishing a continuous path for the trapped "hopping" electrons. Therefore, the plasma density is highest in this region of maximum E x B resulting in very rapid sputtering. This region is called the "race track". The powersupplies in magnetron sputtering may be dc or rf. DC power supplies can be built to supply up to 20 kW, whereas rf power supplies are limited to - 3 kW. Therefore, dc magnetron sputtering can provide higher deposition rates than rf magnetron sputtering, and consequently is more widely used. The distance between the target and the wafer is typically 5 - 10 cm, the operating pressure is - 2 - 10 mtorr and the elecctrode voltage is a few hundred volts. In most cases the wafer is kept at normal room temperature, however, some times heating is also used.

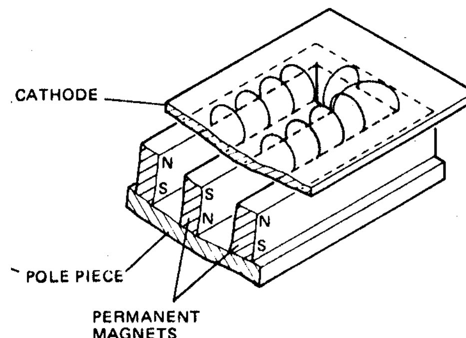
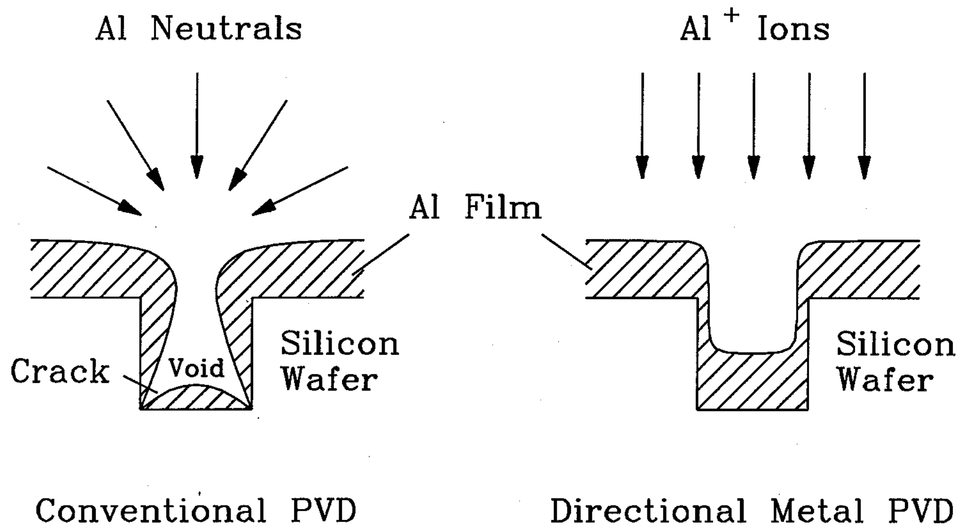


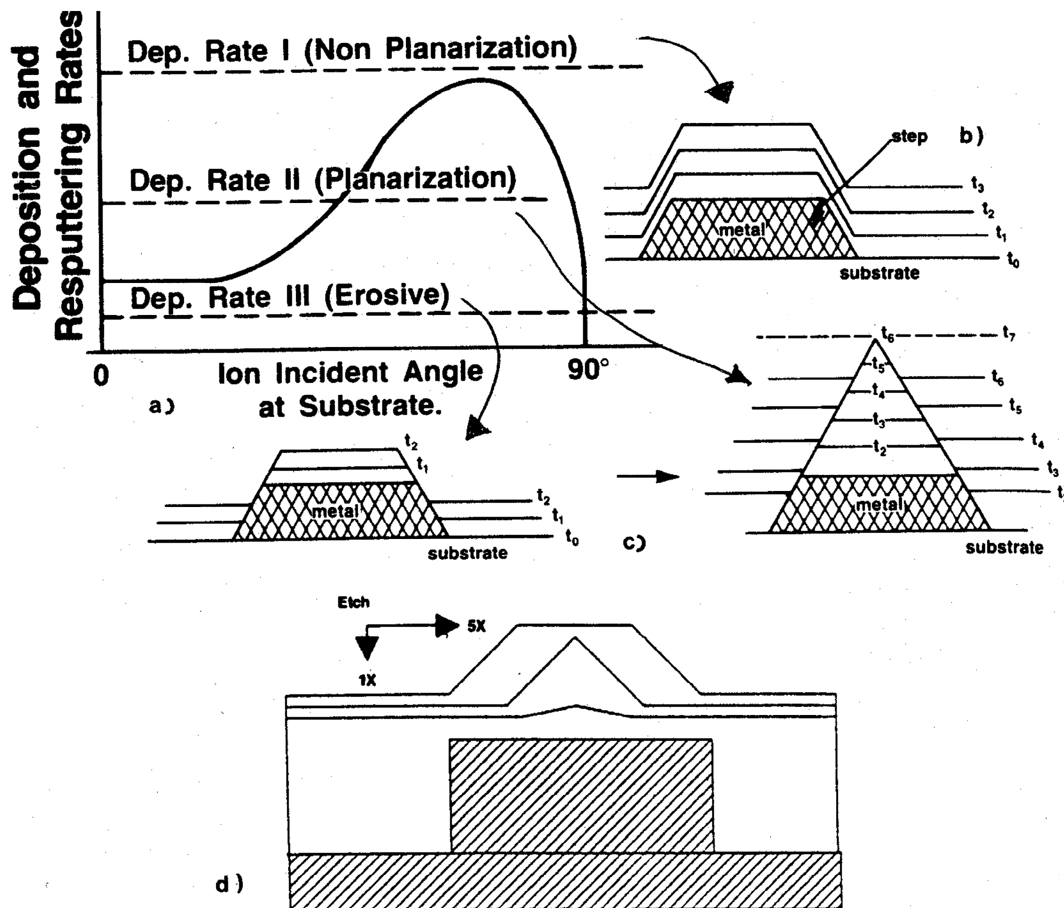
Fig. 12 Schematic diagrams of a planar magnetron target.

Deposition profile in Sputtering



The step coverage can be improved by increasing the surface diffusivity by heating the wafer during or after the deposition.

Bias Sputtering



Degree of planarization

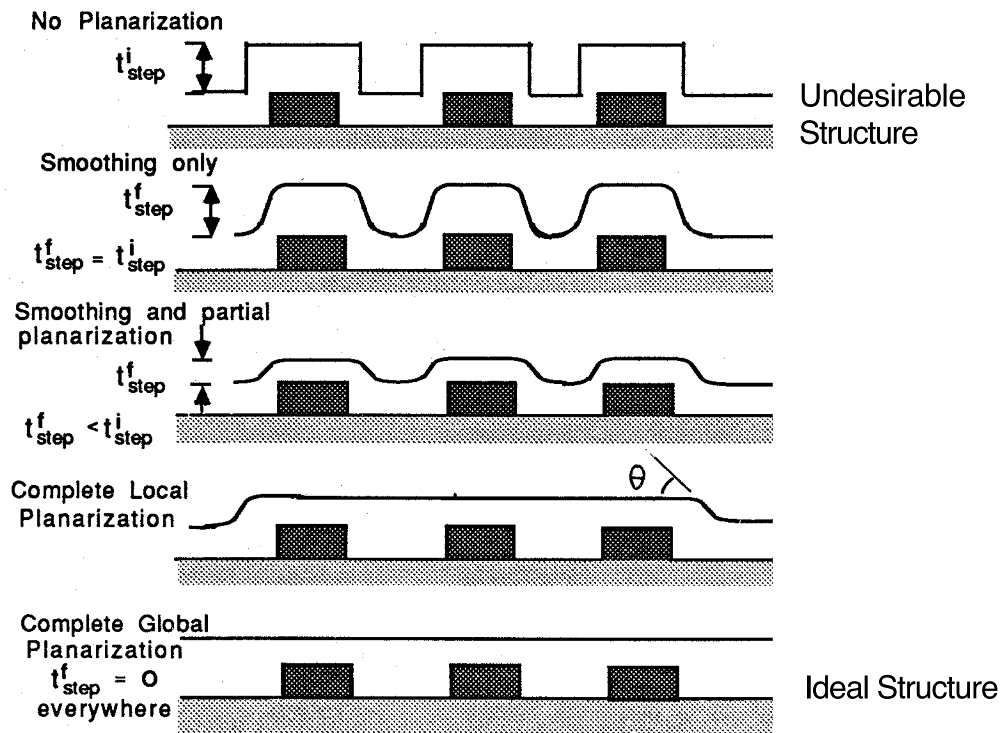


Fig. 4. Degree of Planarization.

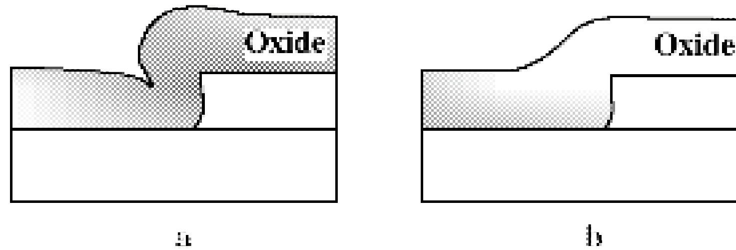
$$\text{Degree of Planarization} = 1 - \frac{t^i_{step}}{t^f_{step}} \qquad \text{slope} = \theta$$

Planarization Methods

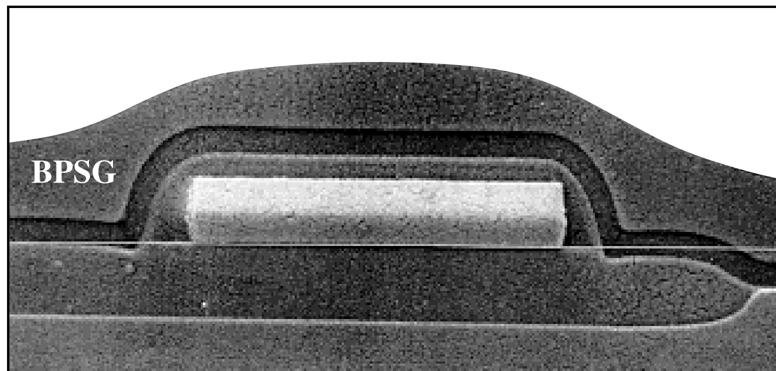
- Reflow of SiO_2 doped with phosphorus and boron glass
- Reflow of metal
- LPCVD of tungsten
- Etch-back of a sacrificial layer
- Simultaneous etch and deposition
- Organic spin coating
- Chemical Mechanical Polishing (CMP)

Reflow of Doped SiO_2 (First level dielectric)

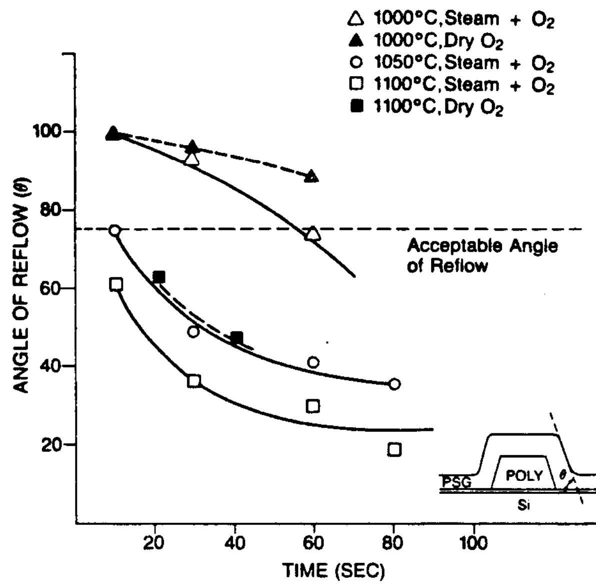
Addition of B_2O_3 and P_2O_5 concurrently further decreases the viscosity. Viscous flow is a strong function of the ambient.

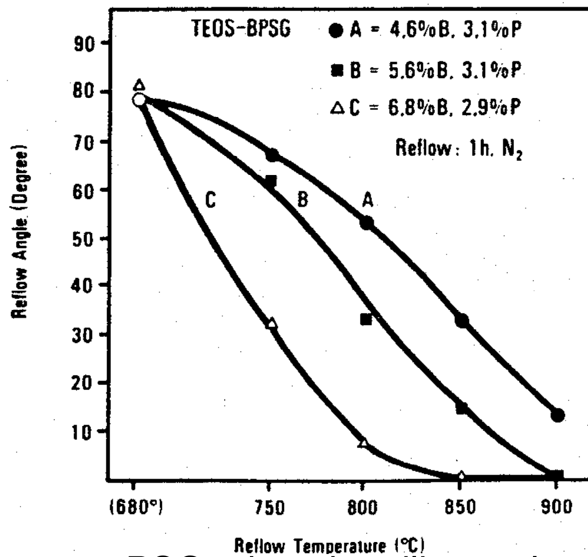


Figures above show topography of silane-based LPCVD oxide layer over a step: a. as-deposited, or annealed with no dopant in oxide; b. after anneal with dopants like phosphorus and boron in oxide, showing reflow.



Above is SEM image of BPSG oxide layer after 800˚C reflow step, showing smooth topography over step.

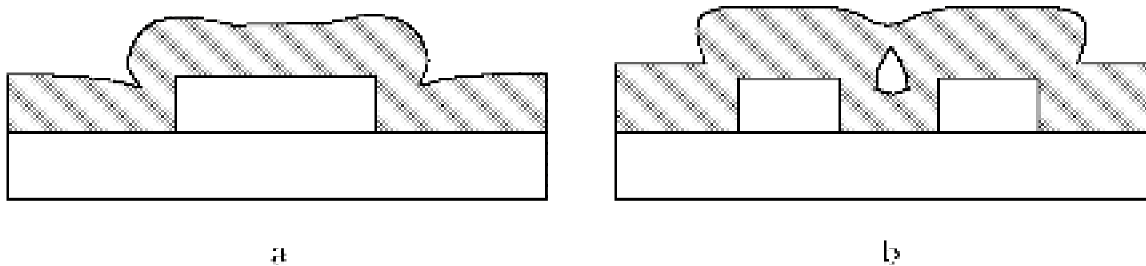




- PSG: phospho-silicate glass, will reflow at 950 - 1100˚C
- BPSG: boro-phospho-silicate glass, will reflow at 800˚C.

Intermetal dielectric are also made of SiO_2, but cannot be subjected to reflow or densification anneals.

• Two common problems occur cusping and voids.



Etchback Planarization Using Sacrificial Layers

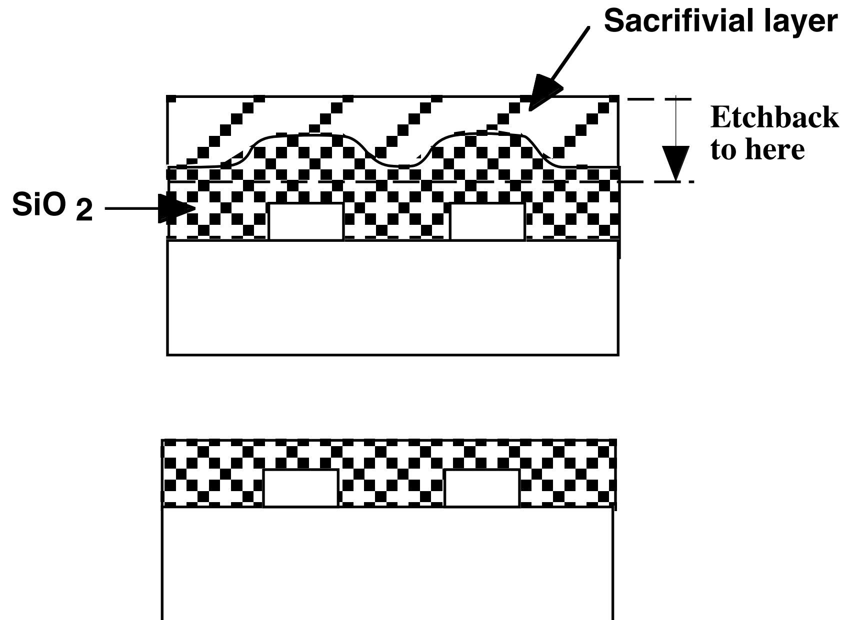
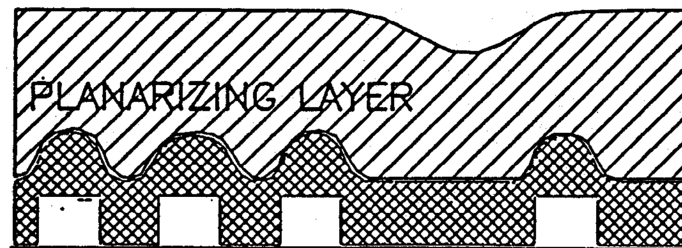


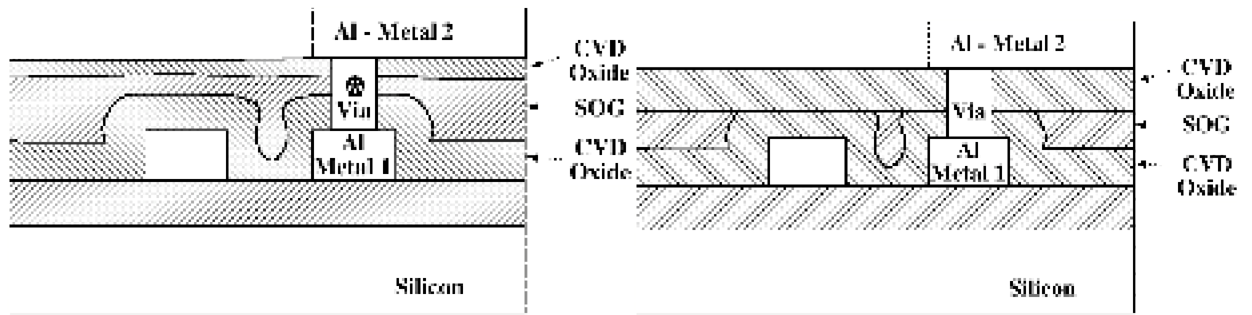
Illustration of photoresist etchback process. Photoresist is deposited over rough topography, then the structure is etchedback, leaving a smooth top surface of the oxide.



More realistic profile due to micro loading resulting in local planarization.

Spin-on-glass (SOG)

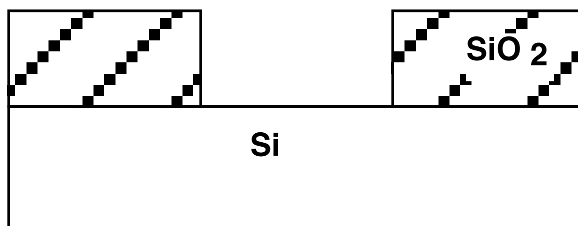
- Fills like liquid photoresist, but becomes SiO_2 after bake and cure.
- Done with or without etchback (with etchback to prevent poisoned via).
- Can also use low-K SOD's. (spin-on-dielectrics)

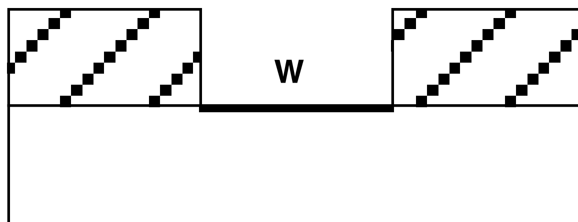


without etchback **with etchback**

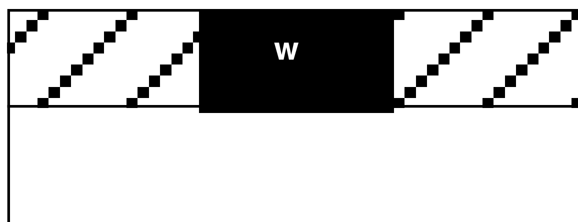
- SOG oxides not as good quality as thermal or CVD oxides
- Use sandwich layers.

Selective CVD of W



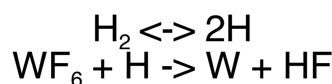


$2WF_6 + 3Si = 2W + 3SiF_4$
Deposition only on Si
Limiting thickness



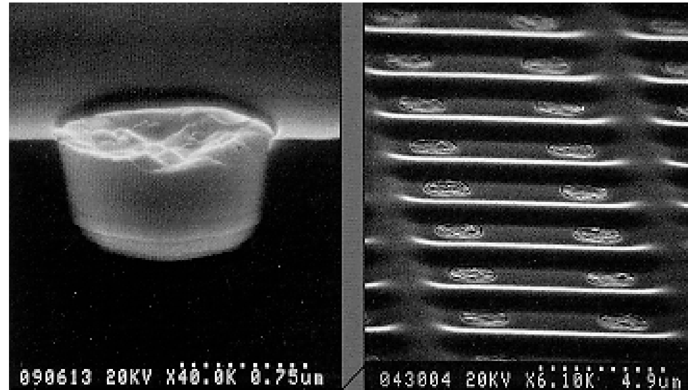
$WF_6 + 3H_2 = W + 6HF$
Deposition only on W

For the hydrogen reduction to occur atomic hydrogen is needed

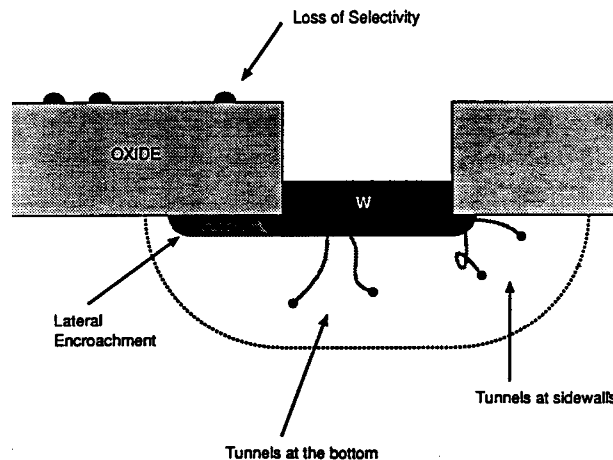


$$H_2 \leftrightarrow 2H$$
$$WF_6 + H \rightarrow W + HF$$

The dissociation of H_2 to H occurs readily on metallic surfaces, but not on dielectric surfaces. Hence the overall deposition is selective.



This technique has been demonstrated for filling vias and many other applications, e.g., strapping of poly-Si and source drain junctions similar to the salicide technology. However, there are many problems which have impeded the acceptance of this technology in manufacturing.



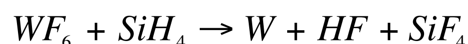
Problems of Selective CVD of W

- Loss of selectivity
- Lateral Encroachment
- Tunnels

The last two problems take place during the initial deposition of W. during the Si reaction with WF_6 any crystal imperfection enhances the reaction. Generally heavily doped regions always have some defects. Loss of selectivity results because of contaminants and dangling bonds.

Non-Selective CVD of W

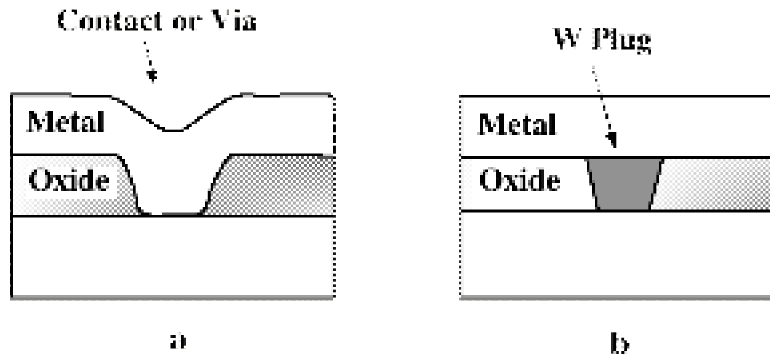
Tungsten can also be deposited by SiH_4 reduction of WF_6, however, the deposition is non selective.



$$WF_6 + SiH_4 \rightarrow W + HF + SiF_4$$

HF and SiF_4 are gaseous byproducts.

• A commonly used planarization technique is the use of W plugs for contacts and vias:



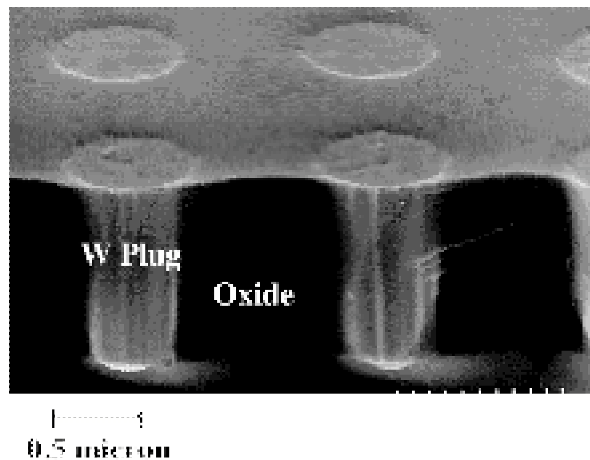
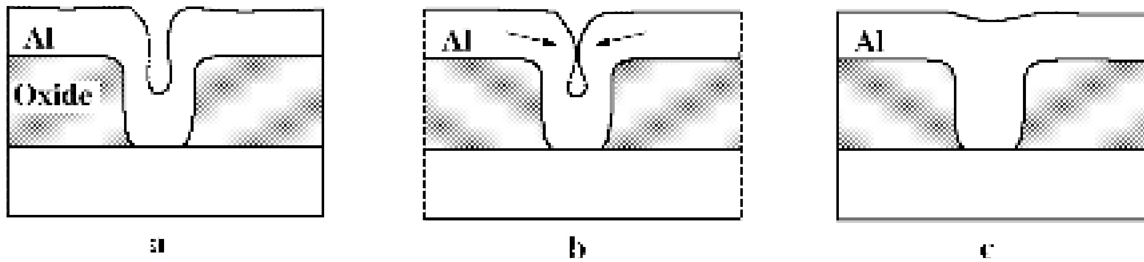


Fig. SEM image of W plugs after blanket CVD deposition and CMP. Photo courtesy of VLSI Technology, Inc.

Generally adhesion of CVD W to SiO_2 is poor. Therefore, a glue layer is used as an adhesion promotor. The best choice is TiN.

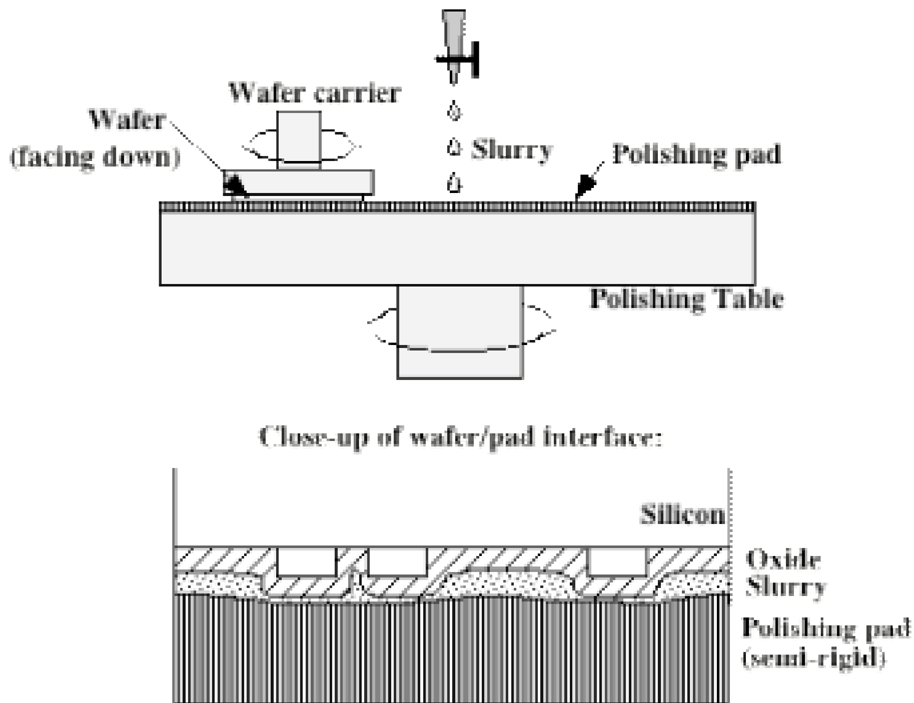
Reflow of Metal

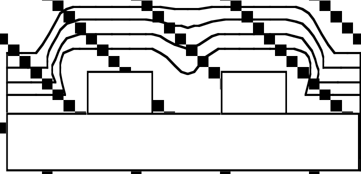
A planarization method that does involve Al as a contact or via material is reflow.



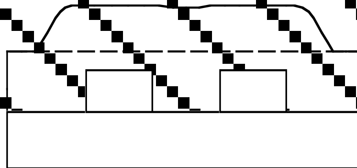
Wafer is heated at 450-550˚C to help fill contact or via and planarize structure. Driving force for reflow is surface energy reduction.

Chemical-Mechanical Polishing (CMP)

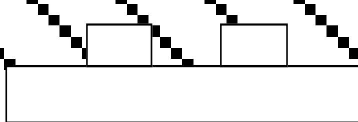




1. deposit thick oxide



2. etch off top



3. globally planarized topography remains

- CMP, once considered a technique too crude and dirty for IC fabrication, is now commonly used.
- Global, or near global, planarization can be achieved.
- Can be used for dielectrics, as well as for metals (W plug, for example).